

# High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter

## FEATURES

- Regulated Output with Input Above, Below or Equal to the Output
- Single Inductor, No Schottky Diodes
- High Efficiency: Up to 96%
- 28 $\mu$ A Quiescent Current in Burst Mode<sup>®</sup> Operation
- Up to 1.2A Continuous Output Current from a Single Lithium-Ion
- True Output Disconnect in Shutdown
- 2.4V to 5.5V Input Range
- 2.4V to 5.25V Output Range
- 600kHz Fixed Frequency Operation
- Synchronizable Oscillator
- Selectable Burst Mode or Fixed Frequency Operation
- <1 $\mu$ A Quiescent Current in Shutdown
- Small, Thermally Enhanced 12-Lead (4mm  $\times$  3mm  $\times$  0.8mm) DFN package

## APPLICATIONS

- Handheld Computers
- Handheld Instruments
- MP3 Players
- Digital Cameras

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## DESCRIPTION

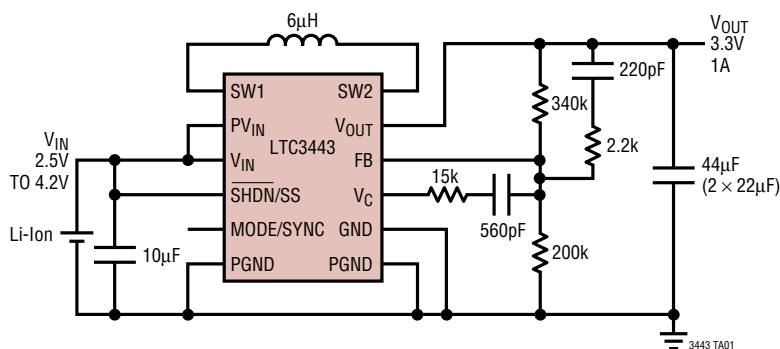
The LTC<sup>®</sup>3443 is a high efficiency, fixed frequency, buck-boost DC/DC converter that operates from input voltages above, below or equal to the output voltage. The part is pin for pin compatible with its predecessor, the LTC3441, with a lower operating frequency (600kHz), and a V<sub>C</sub> pin clamp circuit during Burst Mode operation. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single Lithium Ion or multicell applications where the output voltage is within the battery voltage range.

The device includes two 0.10 $\Omega$  N-channel MOSFET switches and two 0.11 $\Omega$  P-channel switches. External Schottky diodes are optional, and can be used for a moderate efficiency improvement. The operating frequency is internally set to 600kHz and can be synchronized up to 1.2MHz. Quiescent current is only 28 $\mu$ A in Burst Mode operation, maximizing battery life in portable applications. Burst Mode operation is user controlled and can be enabled by driving the MODE/SYNC pin high. If the MODE/SYNC pin is driven low or with a clock, then fixed frequency switching is enabled.

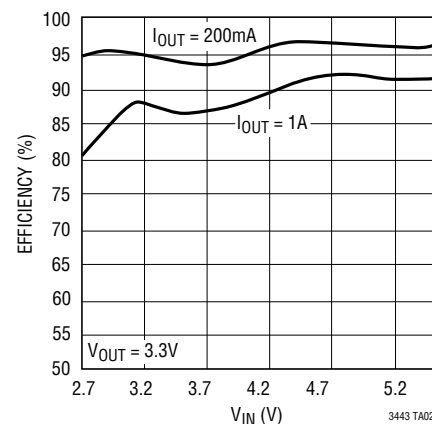
Other features include a 1 $\mu$ A shutdown, soft-start control, thermal shutdown and current limit. The LTC3443 is available in a thermally enhanced 12-lead (4mm  $\times$  3mm) DFN Package.

## TYPICAL APPLICATION

Li-Ion to 3.3V at 1A Buck-Boost Converter



Efficiency vs V<sub>IN</sub>



## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ , $V_{OUT}$ Voltage .....	-0.3V to 6V
SW1, SW2 Voltage	
DC .....	-0.3V to 6V
Pulsed < 100ns .....	-0.3V to 7V
SHDN/SS, MODE/SYNC Voltage .....	-0.3V to 6V
Operating Temperature Range (Note 2) ..	-40°C to 85°C
Maximum Junction Temperature (Note 4) .....	125°C
Storage Temperature Range .....	-65°C to 125°C

## PACKAGE/ORDER INFORMATION

<p>DE12 PACKAGE 12-LEAD (4mm × 3mm) PLASTIC DFN</p> <p><math>T_{JMAX} = 125^{\circ}C</math>  <math>\theta_{JA} = 53^{\circ}C/W</math> 1-LAYER BOARD  <math>\theta_{JA} = 43^{\circ}C/W</math> 4-LAYER BOARD  <math>\theta_{JC} = 4.3^{\circ}C/W</math>          EXPOSED PAD IS PGND (PIN 13)          MUST BE SOLDERED TO PCB</p>	ORDER PART NUMBER
	LTC3443EDE
	DE PART MARKING
	3443
<b>Order Options</b> Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a>	

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{IN} = V_{OUT} = 3.6V$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Start-Up Voltage		●	2.3	2.4	V	
Output Voltage Adjust Range		●	2.4	5.25	V	
Feedback Voltage		●	1.19	1.22	1.25	V
Feedback Input Current	$V_{FB} = 1.22V$		1	50	nA	
Quiescent Current—Burst Mode Operation	$V_C = 0V$ , MODE/SYNC = 3V (Note 3)		28	45	$\mu A$	
Quiescent Current—SHDN	$V_{OUT} = \overline{SHDN} = 0V$ , Not Including Switch Leakage		0.1	1	$\mu A$	
Quiescent Current—Active	MODE/SYNC = 0V (Note 3)		520	900	$\mu A$	
NMOS Switch Leakage	Switches B and C		0.1	7	$\mu A$	
PMOS Switch Leakage	Switches A and D		0.1	10	$\mu A$	
NMOS Switch On Resistance	Switches B and C		0.10		$\Omega$	
PMOS Switch On Resistance	Switches A and D		0.11		$\Omega$	
Input Current Limit		●	2	3.2	A	
Max Duty Cycle	Boost (% Switch C On)	●	70	88	%	
	Buck (% Switch A In)	●	100		%	
Min Duty Cycle		●		0	%	
Frequency Accuracy		●	510	600	690	kHz
MODE/SYNC Threshold		●	0.4	1.4	V	
MODE/SYNC Input Current	$V_{MODE/SYNC} = 5.5V$		0.01	1	$\mu A$	
Error Amp $A_{VOL}$			90		dB	
Error Amp Source Current			14		$\mu A$	
Error Amp Sink Current			300		$\mu A$	

3443fa

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = V_{OUT} = 3.6\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SHDN/SS Threshold	When IC is Enabled	● 0.4	1	1.4	V
SHDN/SS Threshold	When EA is at Max Boost Duty Cycle		2	2.4	V
SHDN/SS Input Current	$V_{\text{SHDN}} = 5.5\text{V}$		0.01	1	$\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3443E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

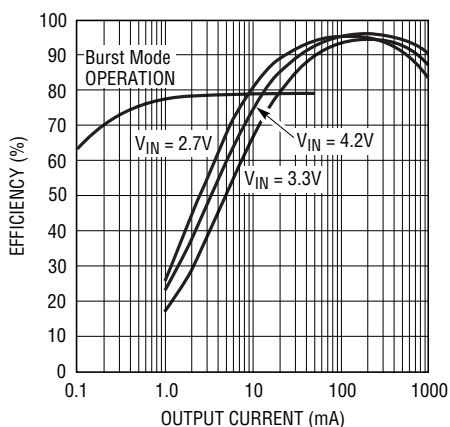
**Note 3:** Current measurements are performed when the outputs are not switching.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

# TYPICAL PERFORMANCE CHARACTERISTICS

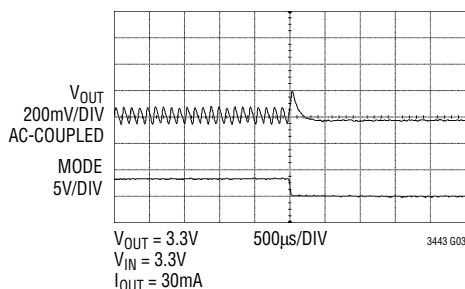
( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Li-Ion to 3.3V Efficiency



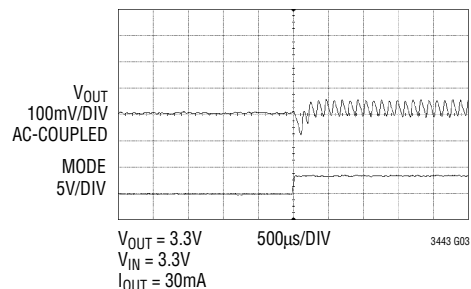
3443 G01

MODE Transient Response: Burst Mode Operation to Fixed Frequency



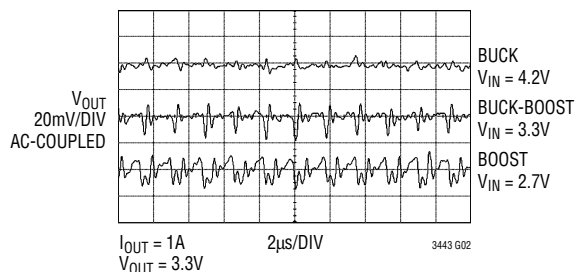
3443 G03

MODE Transient Response: Fixed Frequency to Burst Mode Operation



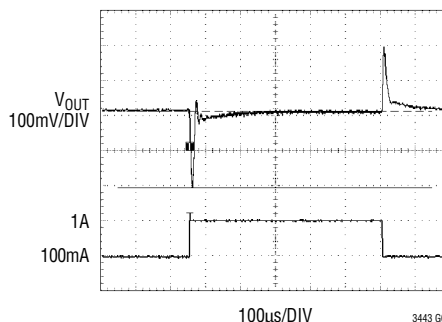
3443 G03

VOUT Ripple at 1A Load



3443 G02

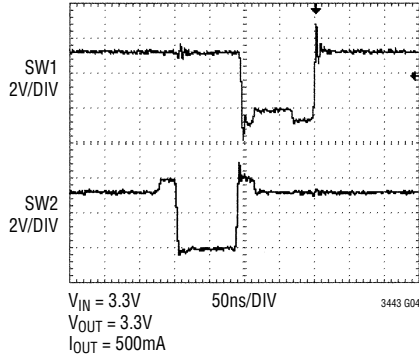
Load Transient Response, 100mA to 1A



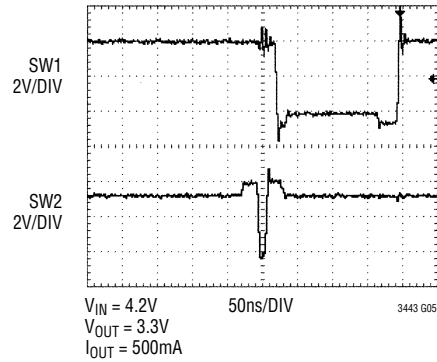
3443 G03

## TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

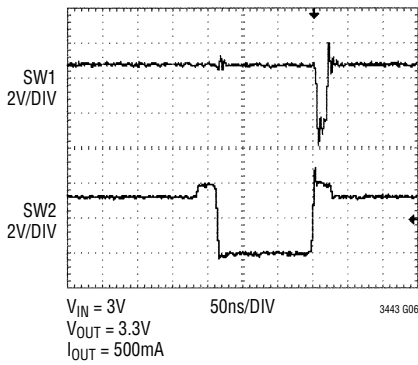
### Switch Pins in Buck-Boost Mode



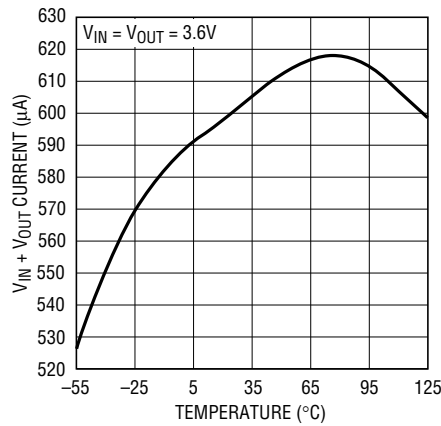
### Switch Pins Entering Buck-Boost Mode



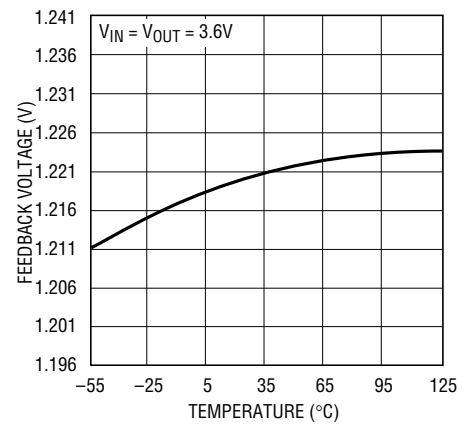
### Switch Pins Before Entering Boost Mode



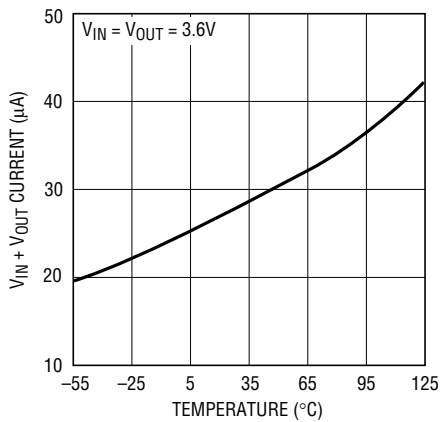
### Active Quiescent Current



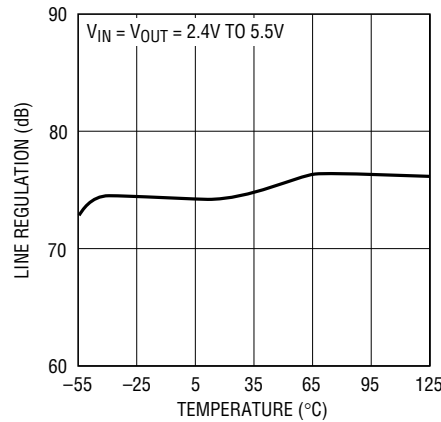
### Feedback Voltage



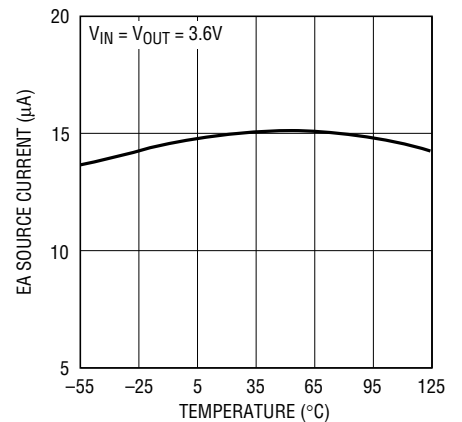
### Burst Mode Quiescent Current



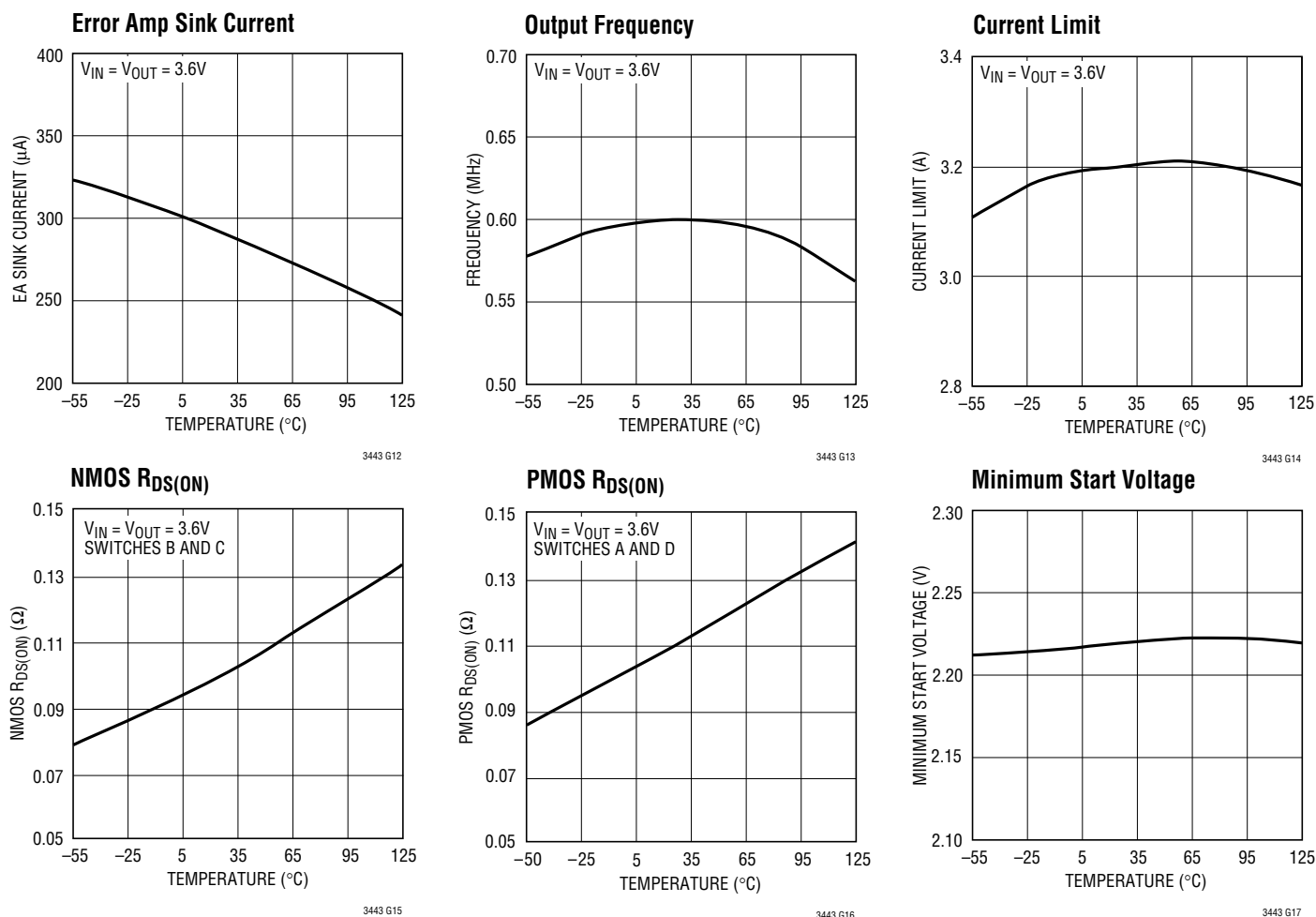
### Feedback Voltage Line Regulation



### Error Amp Source Current



## TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)



## PIN FUNCTIONS

**SHDN/SS (Pin 1):** Combined Soft-Start and Shutdown. Applied voltage  $< 0.4\text{V}$  shuts down the IC. Tie to  $>1.4\text{V}$  to enable the IC and  $>2.4\text{V}$  to ensure the error amp is not clamped from soft-start. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of the  $V_C$  pin.

**GND (Pin 2):** Signal Ground for the IC.

**PGND (Pins 3, 6, 13 Exposed Pad):** Power Ground for the Internal NMOS Power Switches. The exposed pad must be soldered to PCB ground for optimal thermal performance.

**SW1 (Pin 4):** Switch pin where the internal switches A and B are connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from this SW1 to ground. Minimize trace length to keep EMI down.

**SW2 (Pin 5):** Switch pin where the internal switches C and D are connected. An optional Schottky diode can be connected from SW2 to  $V_{OUT}$  (it is required where  $V_{OUT} > 4.3\text{V}$ ). Minimize trace length to keep EMI down.

**MODE/SYNC (Pin 7):** Burst Mode Select and Oscillator Synchronization.

MODE/SYNC = High: Enable Burst Mode Operation. During the period where the IC is supplying energy to the output, the inductor peak inductor current will reach  $0.8\text{A}$  and return to zero current on each cycle. In Burst Mode operation the operation is variable frequency, which provides a significant efficiency improvement at light loads. The Burst Mode operation will continue until the pin is driven low.

## PIN FUNCTIONS

MODE/SYNC = Low: Disable Burst Mode operation and maintain low noise, constant frequency operation .

MODE/SYNC = External CLK : Synchronization of the internal oscillator and Burst Mode operation disable. A clock pulse width between 100ns and 2μs and a clock frequency between 1.38MHz and 2.4MHz (twice the desired frequency) is required to synchronize the IC.

$$f_{OSC} = f_{SYNC}/2$$

**V<sub>OUT</sub> (Pin 8):** Output of the Synchronous Rectifier. A filter capacitor is placed from V<sub>OUT</sub> to GND. A ceramic bypass capacitor is recommended as close to the V<sub>OUT</sub> and GND pins as possible.

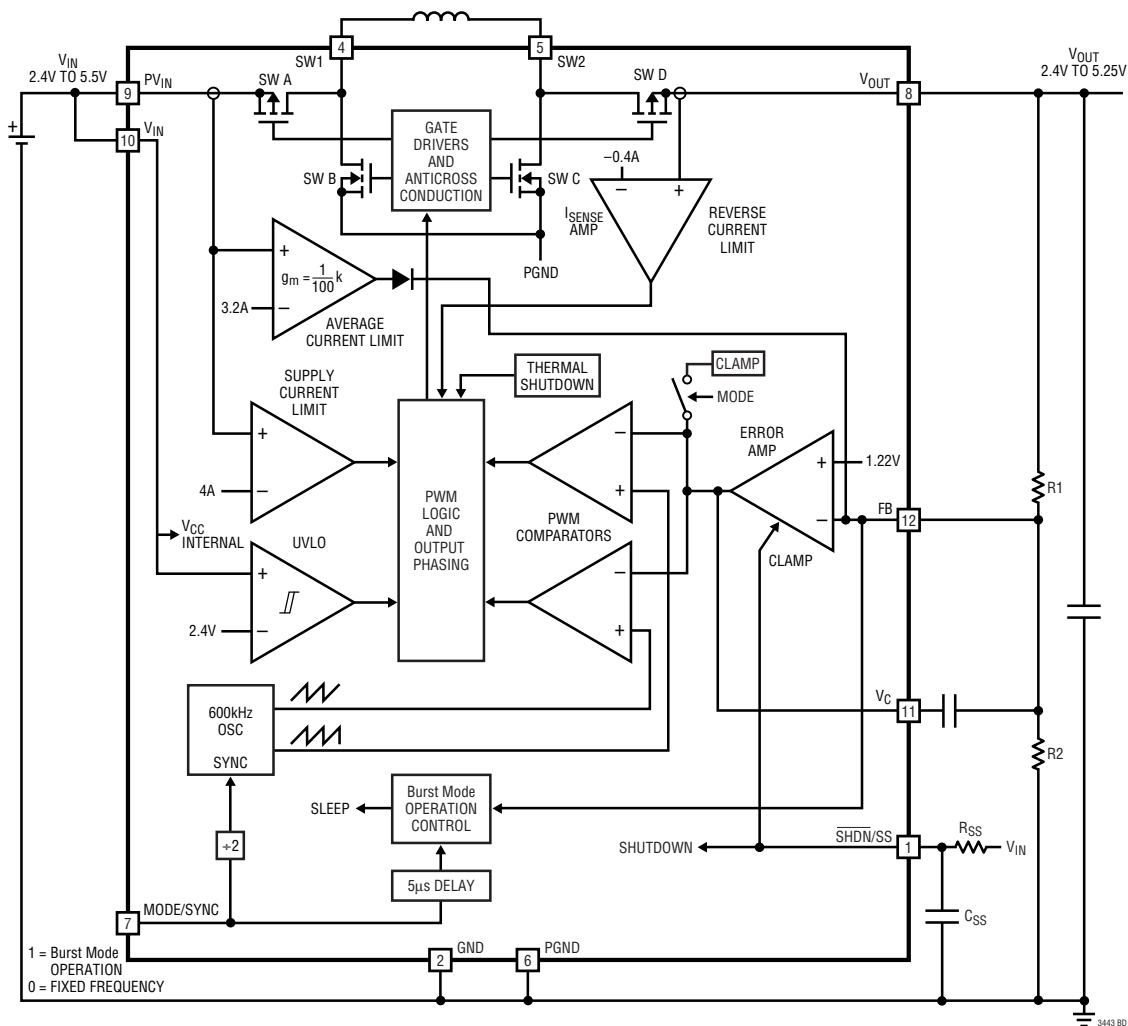
**PV<sub>IN</sub> (Pin 9):** Power V<sub>IN</sub> Supply Pin. A 10μF ceramic capacitor is recommended as close to the PV<sub>IN</sub> and PGND pins as possible

**V<sub>IN</sub> (Pin 10):** Input Supply Pin. Internal V<sub>CC</sub> for the IC.

**V<sub>C</sub> (Pin 11):** Error Amp Output. A frequency compensation network is connected from this pin to the FB pin to compensate the loop. See the section “Compensating the Feedback Loop” for guidelines.

**FB (Pin 12):** Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.4V to 5.25V. The feedback reference voltage is typically 1.22V.

## BLOCK DIAGRAM



## OPERATION

The LTC3443 provides high efficiency, low noise power for applications such as portable instrumentation. The LTC proprietary topology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amp output voltage on the  $V_C$  pin determines the output duty cycle of the switches. Since the  $V_C$  pin is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low  $R_{DS(ON)}$ , low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower drop during the break-before-make time (typically 15ns). The addition of the Schottky diodes will improve peak efficiency by typically 1% to 2%. High efficiency is achieved at light loads when Burst Mode operation is entered and when the IC's quiescent current is a low 28 $\mu$ A.

### LOW NOISE FIXED FREQUENCY OPERATION

#### Oscillator

The frequency of operation is factory trimmed to 600kHz. The oscillator can be synchronized with an external clock applied to the MODE/SYNC pin. A clock frequency of twice the desired switching frequency and with a pulse width of at least 100ns is applied. The oscillator sync range is 690kHz to 1.2MHz (1.38MHz to 2.4MHz sync frequency).

#### Error Amp

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier to obtain stability of the converter. The SHDN/SS pin will clamp the error amp output,  $V_C$ , to provide a soft-start function.

#### Supply Current Limit

The current limit amplifier will shut PMOS switch A off once the current exceeds 4A typical. Before the switch current limit, the average current limit amp (3.2A typical) will source current into the FB pin to drop the output voltage. The current amplifier delay to output is typically 50ns.

#### Reverse Current Limit

The reverse current limit amplifier monitors the inductor current from the output through switch D. Once a negative inductor current exceeds  $-400$ mA typical, the IC will shut off switch D.

#### Output Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor,  $V_{IN}$ ,  $V_{OUT}$  and GND. Figure 2 shows the regions of operation for the LTC3443 as a function of the internal control voltage,  $V_{CI}$ . The  $V_{CI}$  voltage is a level shifted voltage from the output of the error amp ( $V_C$  pin) (see Figure 5). The output switches are properly phased so the transfer between operation modes is continuous, filtered and transparent to the user. When  $V_{IN}$  approaches  $V_{OUT}$  the Buck/Boost region is reached where the conduction time of the four switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

#### Buck Region ( $V_{IN} > V_{OUT}$ )

Switch D is always on and switch C is always off during this mode. When the internal control voltage,  $V_{CI}$ , is above voltage  $V1$ , output A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate

## OPERATION

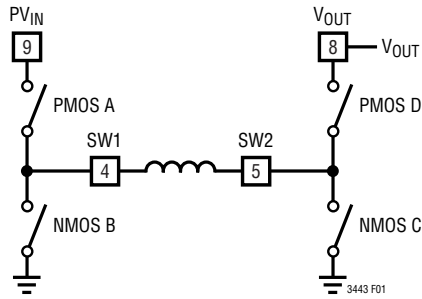


Figure 1. Simplified Diagram of Output Switches

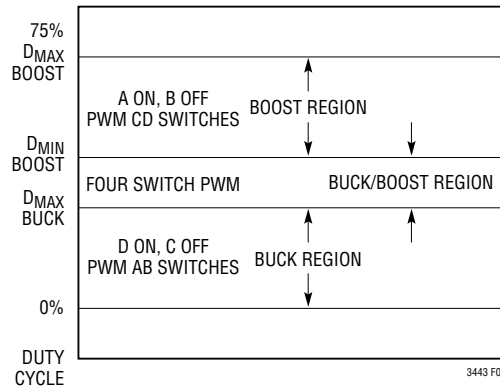


Figure 2. Switch Control vs Internal Control Voltage, V<sub>C1</sub>



## OPERATION

similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in Buck mode reaches  $D_{MAX\_BUCK}$ , given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW} \%$$

where  $D4_{SW}$  = duty cycle % of the four switch range.

$$D4_{SW} = (150ns \cdot f) \cdot 100 \%$$

where  $f$  = operating frequency, Hz.

Beyond this point the “four switch,” or Buck/Boost region is reached.

### Buck/Boost or Four Switch ( $V_{IN} \sim V_{OUT}$ )

When the internal control voltage,  $V_{CI}$ , is above voltage  $V2$ , switch pair AD remain on for duty cycle  $D_{MAX\_BUCK}$ , and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the  $V_{CI}$  voltage reaches the edge of the Buck/Boost range, at voltage  $V3$ , the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle  $D4_{SW}$ .

The input voltage,  $V_{IN}$ , where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1 - (150ns \cdot f)} V$$

The point at which the four switch region ends is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 150ns \cdot f) V$$

### Boost Region ( $V_{IN} < V_{OUT}$ )

Switch A is always on and switch B is always off during this mode. When the internal control voltage,  $V_{CI}$ , is above voltage  $V3$ , switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 88% typical and is reached when  $V_{CI}$  is above  $V4$ .

### Burst Mode OPERATION

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 28 $\mu$ A. In this mode the output ripple has a variable frequency component that depends upon load current.

During the period where the device is delivering energy to the output, the peak current will be equal to 800mA typical and the inductor current will terminate at zero current for each cycle. In this mode the typical maximum average output current is given by:

$$I_{OUT(MAX)BURST} \approx \frac{0.2 \cdot V_{IN}}{V_{OUT} + V_{IN}} A$$

Burst Mode operation is user controlled, by driving the MODE/SYNC pin high to enable and low to disable.

The peak efficiency during Burst Mode operation is less than the peak efficiency during fixed frequency because the part enters full-time 4-switch mode (when servicing the output) with discontinuous inductor current as illustrated in Figures 3 and 4. During Burst Mode operation, the control loop is nonlinear and cannot utilize the control voltage from the error amp to determine the control mode, therefore full-time 4-switch mode is required to maintain the Buck/Boost function. The efficiency below 1mA becomes dominated primarily by the quiescent current and not the peak efficiency. The equation is given by:

$$\text{Efficiency Burst} \approx \frac{(\eta_{bm}) \cdot I_{LOAD}}{25\mu A + I_{LOAD}}$$

where  $(\eta_{bm})$  is typically 80% during Burst Mode operation.

## OPERATION

### SOFT-START

The soft-start function is combined with shutdown. When the SHDN/SS pin is brought above typically 1V, the IC is enabled but the EA duty cycle is clamped from the  $V_C$  pin.

A detailed diagram of this function is shown in Figure 5. The components  $R_{SS}$  and  $C_{SS}$  provide a slow ramping voltage on the SHDN/SS pin to provide a soft-start function.

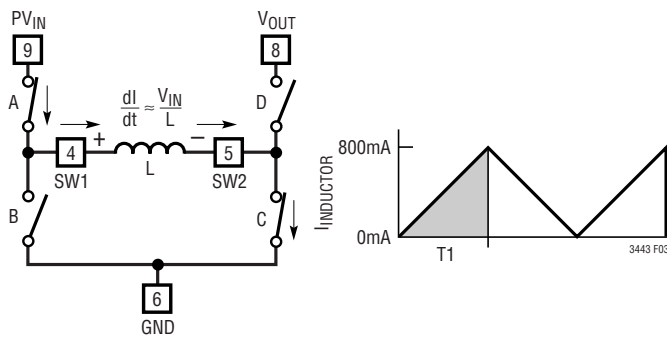


Figure 3. Inductor Charge Cycle During Burst Mode Operation

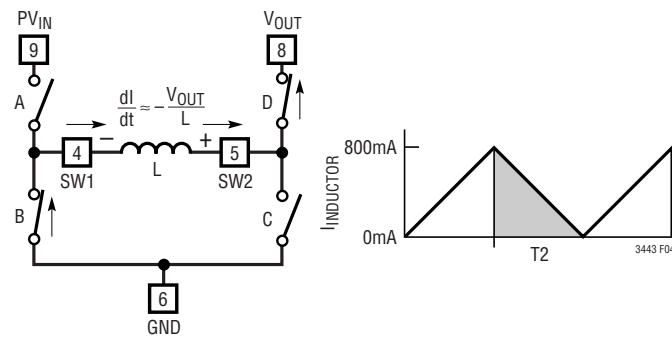


Figure 4. Inductor Discharge Cycle During Burst Mode Operation

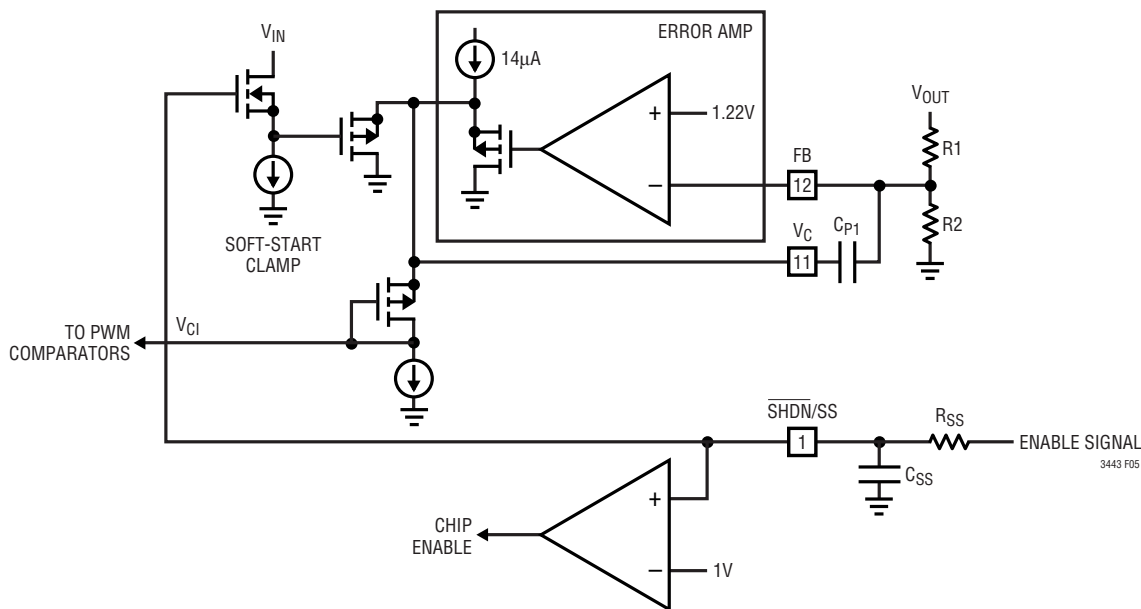
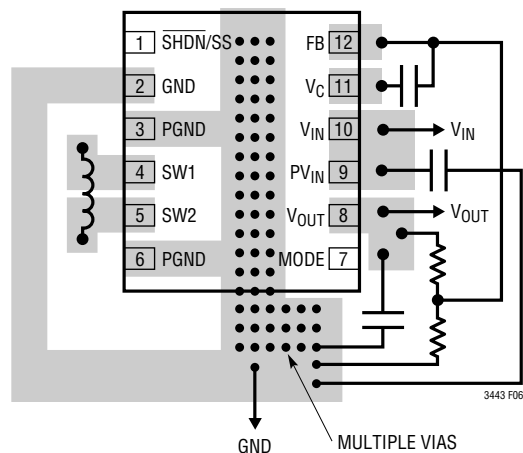


Figure 5. Soft-Start Circuitry

## APPLICATIONS INFORMATION

### COMPONENT SELECTION



**Figure 6. Recommended Component Placement. Traces Carrying High Current are Direct. Trace Area at FB and VC Pins are Kept Low. Lead Length to Battery Should be Kept Short. V<sub>OUT</sub> and V<sub>IN</sub> Ceramic Capacitors Close to the IC Pins**

### Inductor Selection

The high frequency operation of the LTC3443 allows the use of small surface mount inductors. The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L > \frac{V_{IN(MIN)} \cdot (V_{OUT} - V_{IN(MIN)}) \cdot 100}{f \cdot I_{OUT(MAX)} \cdot \%Ripple \cdot V_{OUT}} \text{ H,}$$

$$L > \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT}) \cdot 100}{f \cdot I_{OUT(MAX)} \cdot \%Ripple \cdot V_{IN(MAX)}} \text{ H}$$

where  $f$  = operating frequency, Hz

%Ripple = allowable inductor current ripple, %

$V_{IN(MIN)}$  = minimum input voltage, V

$V_{IN(MAX)}$  = maximum input voltage, V

$V_{OUT}$  = output voltage, V

$I_{OUT(MAX)}$  = maximum output load current

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the  $I^2R$  losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for suggested components and Table 2 for a list of component suppliers.

**Table 1. Inductor Vendor Information**

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(561) 241-7876	(561) 241-9339	www.coiltronics.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	(847) 956-0702 81(3) 3607-5144	www.japanlink.com/ sumida

### Output Capacitor Selection

The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%Ripple\_Boost = \frac{I_{OUT(MAX)} \cdot (V_{OUT} - V_{IN(MIN)}) \cdot 100}{C_{OUT} \cdot V_{OUT}^2 \cdot f} \%$$

$$\%Ripple\_Buck = \frac{I_{OUT(MAX)} \cdot (V_{IN(MAX)} - V_{OUT}) \cdot 100}{C_{OUT} \cdot V_{IN(MAX)} \cdot V_{OUT} \cdot f} \%$$

where  $C_{OUT}$  = output filter capacitor, F

The output capacitance is usually many times larger in order to handle the transient response of the converter. For a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the

## APPLICATIONS INFORMATION

above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended.

### Input Capacitor Selection

Since the  $V_{IN}$  pin is the supply voltage for the IC it is recommended to place at least a 4.7 $\mu$ F, low ESR bypass capacitor.

**Table 2. Capacitor Vendor Information**

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

### Optional Schottky Diodes

The Schottky diodes across the synchronous switches B and D are not required ( $V_{OUT} < 4.3V$ ), but provide a lower drop during the break-before-make time (typically 15ns) of the NMOS to PMOS transition, improving efficiency. Use a Schottky diode such as a Phillips PMEG2010EA or equivalent. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. For applications with an output voltage above 4.3V, a Schottky diode is required from SW2 to  $V_{OUT}$ .

### Output Voltage < 2.4V

The LTC3443 can operate as a buck converter with output voltages as low as 0.4V. The part is specified at 2.4V minimum to allow operation without the requirement of a Schottky diode. Synchronous switch D is powered from  $V_{OUT}$  and the  $R_{DS(ON)}$  will increase at low output voltages, therefore a Schottky diode is required from SW2 to  $V_{OUT}$  to provide the conduction path to the output.

### Output Voltage > 4.3V

A Schottky diode from SW to  $V_{OUT}$  is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to the parasitic lead and trace inductance.

### Input Voltage > 4.5V

For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a 2 $\Omega$ /1nF series snubber is required between the SW1 pin and GND. A Schottky diode from SW1 to  $V_{IN}$  should also be added as close to the pins as possible. For the higher input voltages,  $V_{IN}$  bypassing becomes more critical; therefore, a ceramic bypass capacitor as close to the  $V_{IN}$  and GND pins as possible is also required.

### Operating Frequency Selection

Additional quiescent current due to the output switches GATE charge is given by:

$$\text{Buck: } 800e^{-12} \cdot V_{IN} \cdot f$$

$$\text{Boost: } 400e^{-12} \cdot (V_{IN} + V_{OUT}) \cdot f$$

$$\text{Buck/Boost: } f \cdot (1200e^{-12} \cdot V_{IN} + 400e^{-12} \cdot V_{OUT})$$

where  $f$  = switching frequency

### Closing the Feedback Loop

The LTC3443 incorporates voltage mode PWM control. The control to output gain varies with operation region (Buck, Boost, Buck/Boost), but is usually no greater than 15. The output filter exhibits a double pole response is given by:

$$f_{\text{FILTER\_POLE}} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \text{ Hz}$$

where  $C_{OUT}$  is the output filter capacitor.

## APPLICATIONS INFORMATION

The output filter zero is given by:

$$f_{\text{FILTER\_ZERO}} = \frac{1}{2 \cdot \pi \cdot R_{\text{ESR}} \cdot C_{\text{OUT}}} \text{ Hz}$$

where  $R_{\text{ESR}}$  is the capacitor equivalent series resistance.

A troublesome feature in Boost mode is the right-half plane zero (RHP), and is given by:

$$f_{\text{RHPZ}} = \frac{V_{\text{IN}}^2}{2 \cdot \pi \cdot I_{\text{OUT}} \cdot L \cdot V_{\text{OUT}}} \text{ Hz}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop requires to be crossed over a decade before the LC double pole.

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{\text{UG}} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{\text{P1}}} \text{ Hz}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate for the double-pole response.

$$f_{\text{POLE1}} \approx \frac{1}{2 \cdot \pi \cdot 32e^3 \cdot R_1 \cdot C_{\text{P1}}} \text{ Hz}$$

Which is extremely close to DC

$$f_{\text{ZERO1}} = \frac{1}{2 \cdot \pi \cdot R_Z \cdot C_{\text{P1}}} \text{ Hz}$$

$$f_{\text{ZERO2}} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{\text{Z1}}} \text{ Hz}$$

$$f_{\text{POLE2}} = \frac{1}{2 \cdot \pi \cdot R_Z \cdot C_{\text{P2}}} \text{ Hz}$$

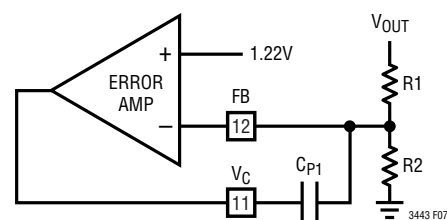


Figure 7. Error Amplifier with Type I Compensation

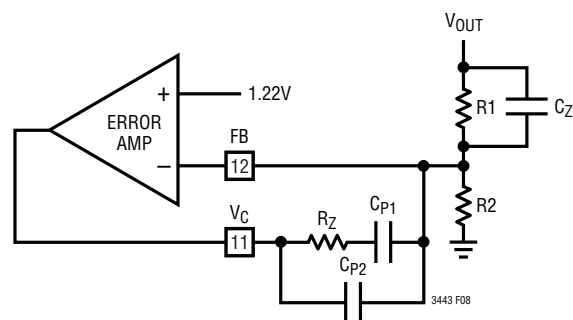
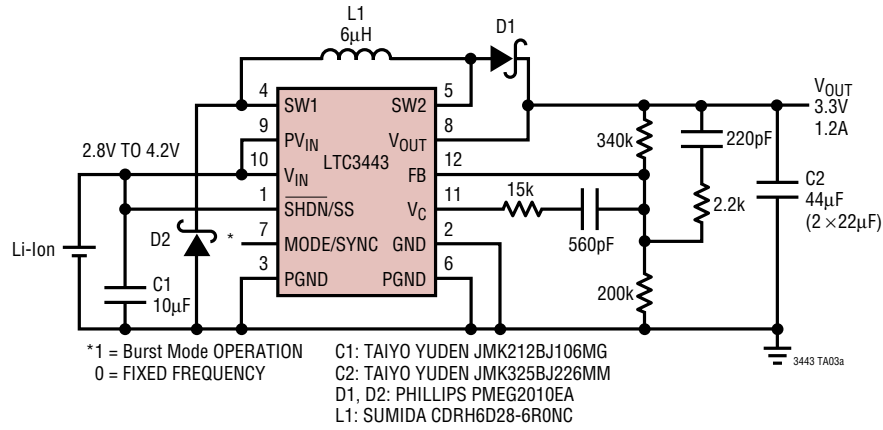


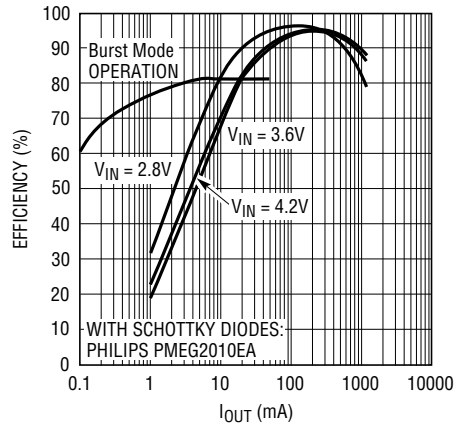
Figure 8. Error Amplifier with Type III Compensation

## TYPICAL APPLICATIONS

### Li-Ion to 3.3V at 1.2A Converter

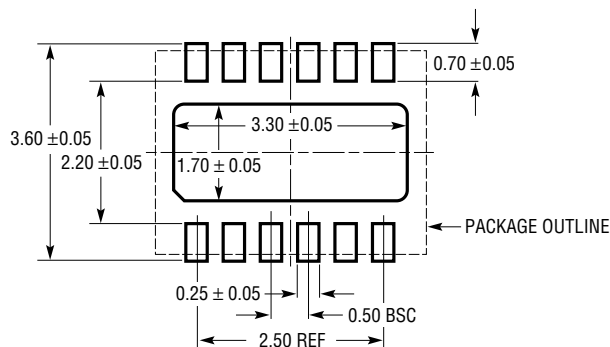


### Efficiency vs Load

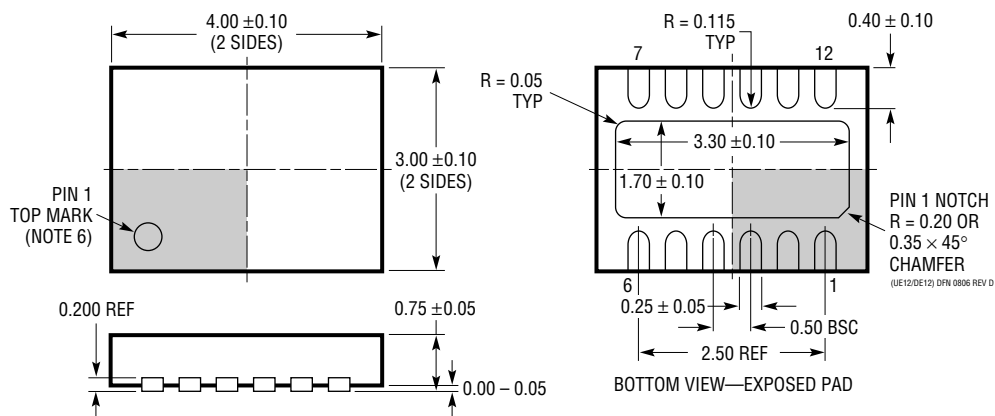


## PACKAGE DESCRIPTION

**DE/UE Package**  
**12-Lead Plastic DFN (4mm × 3mm)**  
 (Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



**NOTE:**

1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT <sup>®</sup> 1613	550mA ( $I_{SW}$ ) 1.4MHz High Efficiency Step-Up DC/DC Converter	$V_{IN}$ : 0.9V to 10V, $V_{OUT(MAX)}$ = 34V, $I_Q$ = 3mA, $I_{SD} \leq 1\mu A$ , ThinSOT <sup>™</sup>
LT1616	500mA ( $I_{OUT}$ ) 1.4MHz High Efficiency Step-Down DC/DC Converter	High Efficiency, $V_{IN}$ : 3.6V to 25V, $V_{OUT(MIN)}$ = 1.25V, $I_Q$ = 1.9mA, $I_{SD} \leq 1\mu A$ , ThinSOT
LTC1776	500mA ( $I_{OUT}$ ) 200kHz High Efficiency Step-Down DC/DC Converter	High Efficiency, $V_{IN}$ : 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, $I_Q$ = 3.2mA, $I_{SD} \leq 30\mu A$ , N8, S8
LTC1877	600mA ( $I_{OUT}$ ) 550kHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.7V to 10V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 10 $\mu A$ , $I_{SD} \leq 1\mu A$ , MS8
LTC1878	600mA ( $I_{OUT}$ ) 550kHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 10 $\mu A$ , $I_{SD} \leq 1\mu A$ , MS8
LTC1879	1.2A ( $I_{OUT}$ ) 550kHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.7V to 10V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 15 $\mu A$ , $I_{SD} \leq 1\mu A$ , TSSOP16
LT1930/LT1930A	1A ( $I_{SW}$ ) 1.2MHz/2.2MHz High Efficiency Step-Up DC/DC Converter	$V_{IN}$ 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, $I_Q$ = 5.5mA, $I_{SD} \leq 1\mu A$ , ThinSOT
LTC3405/LTC3405A	300mA ( $I_{OUT}$ ) 1.5MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 20 $\mu A$ , $I_{SD} \leq 1\mu A$ , ThinSOT
LTC3406/LTC3406B	600mA ( $I_{OUT}$ ) 1.5MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 20 $\mu A$ , $I_{SD} \leq 1\mu A$ , ThinSOT
LTC3407	600mA ( $I_{OUT}$ ) $\times 2$ 1.5MHz Dual Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40 $\mu A$ , $I_{SD} \leq 1\mu A$ , 10-Lead MS
LTC3411	1.25A ( $I_{OUT}$ ) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60 $\mu A$ , $I_{SD} \leq 1\mu A$ , 10-Lead MS
LTC3412	2.5A ( $I_{OUT}$ ) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60 $\mu A$ , $I_{SD} \leq 1\mu A$ , TSSOP16E
LTC3440	600mA ( $I_{OUT}$ ) 2MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, $I_Q$ = 25 $\mu A$ , $I_{SD} \leq 1\mu A$ , 10-Lead MS
LTC3441	High Current Micropower 1MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN}$ : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, $I_Q$ = 25 $\mu A$ , $I_{SD} \leq 1\mu A$ , DFN

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